

## A Discrete, Low Phase Noise, 125 MHz Crystal Oscillator for the AD9850 Complete Direct Digital Synthesizer

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The AD9850 complete direct digital synthesizer (DDS) is a popular device used to implement a low cost, high speed, digital synthesis system. Clocking the AD9850 at its maximum rate of 125 MHz may present some technical challenges especially in applications where the phase noise of the sine output is a major concern. Numerous requests for recommended high speed clocking solutions to drive the AD9850 have prompted this application note.

Inexpensive commercial sources for a 125 MHz CMOS clock oscillator to drive the AD9850 are not readily available. One clock oscillator that suits the AD9850 Evaluation Board is made by Champion Technologies (Model K1300, approximately \$45). This is a simple and easily implemented clock source, but it may be cost prohibitive and, generally speaking, these clock oscillators are not known for outstanding phase noise performance.

The discretely implemented Butler oscillator\* circuit (see Figure 1) is a less expensive alternative clock source that has relatively good phase noise performance compared to the typical clock oscillator. The implementation of a Butler oscillator circuit described below uses a single supply (+5 V), incorporates a TTL output stage, and has a parts cost of \$20 to \$25. This solution represents a good compromise among low phase noise performance, circuit complexity, and cost.

Reference oscillator phase noise, in conjunction with the residual phase noise of the AD9850, constitutes the total phase noise of the DDS output signal. Residual phase noise of the AD9850 at 1 kHz offset from a 5 MHz carrier with a 125 MHz reference clock is -134 dBc. DDS, by virtue of its frequency division characteristic, will reduce the reference oscillator's phase noise contribution by

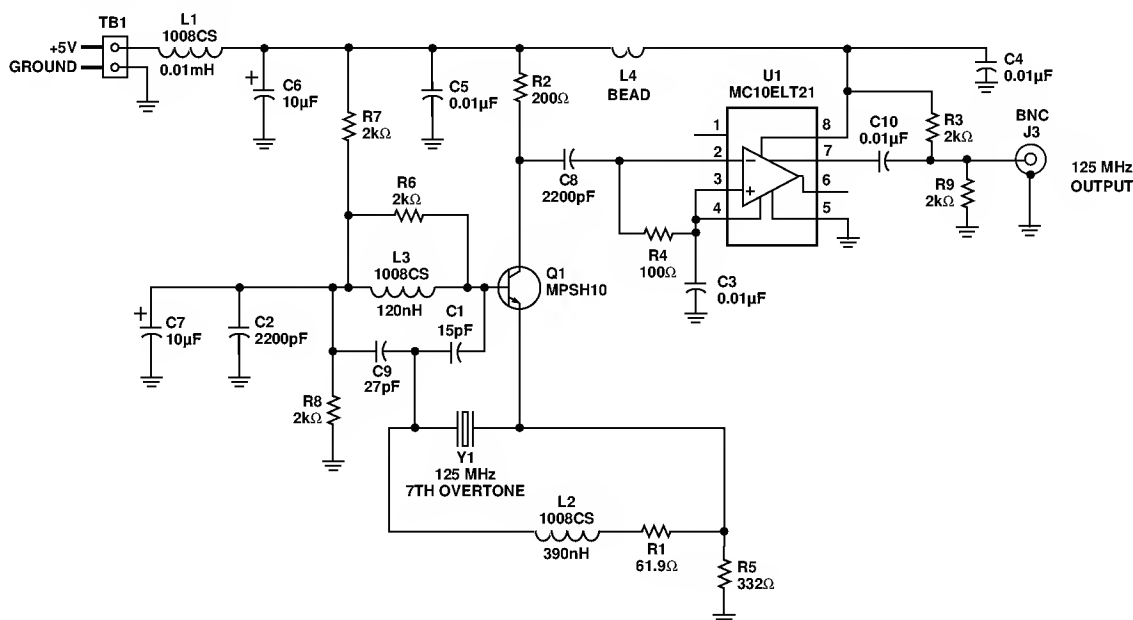


Figure 1. Schematic Diagram and Parts List

\*Butler oscillator circuit provided by Steven Swift, P.E., of Novatech Instruments, Inc., Seattle, Washington. 206/322-1562. <http://www.eskimo.com/~ntsales>

20 LOG (Output Frequency/Reference Frequency). For example, the Butler oscillator's phase noise contribution to the AD9850 output signal is reduced from a typical  $-110$  dBc to  $-138$  dBc when clocking at 125 MHz and outputting 5 MHz. As the DDS output frequency becomes a greater percentage of the reference oscillator frequency, the oscillator's contribution to the DDS output phase noise will increase.

The prototype clock oscillator is built on a  $2" \times 2"$  double-sided copper clad board (Figures 2 and 3). The output will drive 2 V p-p into a  $50\ \Omega$  load and slightly less than 4 V p-p (Figure 4) into a high impedance load. Chip capacitors, chip resistors and chip inductors are used throughout. Q1 can be practically any high frequency NPN with an  $F_T$  3 to 5 times greater than the oscillation frequency—MPS918 and MPSH10 are representative choices. The crystal is seventh overtone, series resonant mode, in an HC-49 holder. U1, the PECL (positive ECL logic) to TTL translator, is a Motorola ECLinPS "Lite" (single gate) surface mount device. U1 will provide

standard TTL output levels or, in this case, CMOS compatible levels that have been externally level-shifted to  $1/2$  the supply voltage of the AD9850. Proper clocking of the AD9850 occurs when the signal is at least 3 V p-p and centered at  $V_{DD}/2$ .

Circuit description: L2/R1 resonate with the crystal stray capacitance to prevent spurious oscillations. The tank circuit containing L3 is resonant near 125 MHz to allow the crystal to operate at its seventh overtone series resonant frequency. R6 reduces the tank circuit Q and prevents self-oscillation and frequency misalignment with the crystal frequency. The MC10ELT21 PECL to TTL translator output is ac-coupled to the midpoint voltage of 2.5 V set up by R3 and R9. The translator requires  $>200$  mV p-p signal input to produce TTL output levels. The oscillator output configuration requires a high load impedance to maintain the 2.5 V dc offset and 4 V signal swing to drive the CMOS input of the AD9850. If actual TTL levels are desired, C10, R3 and R9 should be removed and a wire jumper soldered in place of C10.

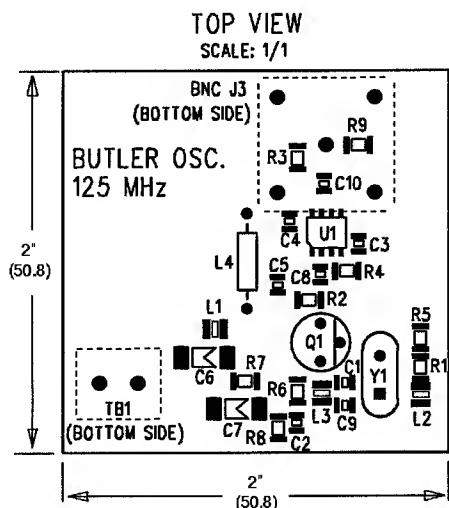


Figure 2. PCB Component Placement

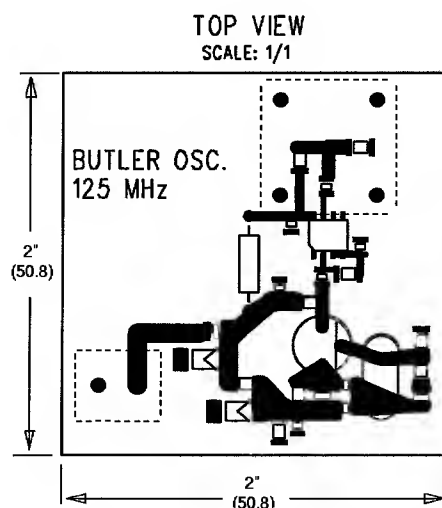


Figure 3. PCB Interconnections

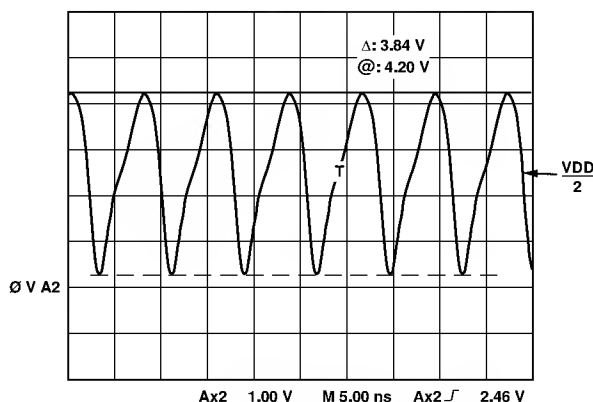


Figure 4. Digital Scope Printout of Oscillator Output